TE0725 HyperRAM

Revision v.9

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Online version of this document:

https://wiki.trenz-electronic.de/pages/viewpage.action?pageId=162172554

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4 Overview

MicroBlaze Design with HyperRAM memory test example.

This reference design is bundled with a FREE evaluation edition of the low-cost, commercially proven, high performance memory controller IP supplied by Synaptic Laboratories Ltd[1] (SLL). This free IP evaluation license never expires, and no customer registration or NIC ID is required. Click here[2] to find the latest free trials of SLL's memory controller IP for HyperBus, OctaBus, Xccela Bus, JEDEC xSPI Profile 1.0 and JEDEC xSPI Profile 2.0 for Intel, Microchip, and Xilinx FPGA. SLL IP is also qualified for use with Trenz HS CRUVI enabled boards. Please send all sales enquiry and technical support questions for SLL's IP to info@synaptic-labs.com[3]

Refer to http://trenz.org/te0725-info for the current online version of this manual and other available documentation.

4.1 Key Features

- Vivado/Vitis 2019.2
- MicroBlaze
- QSPI
- I2C
- UART
- HyperRAM
- S/Labs HBMC IP (Free Trail IP)

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2020-04-29	2019.2	TE0725-HyperRAM_noprebuilt-vivado_2019.2-build_10_20200429134457.zip TE0725-HyperRAM-vivado_2019.2-build_10_20200429134447.zip	John Hartfiel	• add srec application wich loads hello_te0725 from qspi into hyperam
2020-04-17	2019.2	TE0725-HyperRAM-vivado_2019.2-build_10_20200427163950.zip TE0725-HyperRAM_noprebuilt-vivado_2019.2-build_10_20200427163959.zip	John Hartfiel	• 2019.2 update

1 http://synaptic-labs.com/
2 http://synaptic-labs.com/free-trial/memory-controller-ip-for-trenz
3 mailto:info@synaptic-labs.com

Date	Vivado	Project Built	Authors	Description
2018-08-09	2018.2	TE0725-HyperRAM_noprebuilt-vivado_2018.2-build_02_20180809122634.zip TE0725-HyperRAM-vivado_2018.2-build_02_20180809122623.zip	John Hartfiel	• 2018.2 update • new HBMC IP version (v1_3_57)
2018-06-05	2017.4	TE0725-HyperRAM_noprebuilt-vivado_2017.4-build_10_20180605162539.zip TE0725-HyperRAM-vivado_2017.4-build_10_20180605162425.zip	John Hartfiel	• initial release

Table 1: Design Revision History

4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2019.2	needed, Vivado is included into Vitis installation

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.[4]

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

4 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0725-03-15-1C	15_1c	REV03|REV02|REV01	NA	32MB	NA	8MB HypeRAM	NA
TE0725-03-35-2C	35_2c	REV03|REV02|REV01	NA	32MB	NA	8MB HypeRAM	NA
TE0725-03-100-2C	100_2c	REV03|REV02|REV01	NA	32MB	NA	8MB HypeRAM	NA
TE0725-03-100-2CF	100_2c	REV03|REV02|REV01	NA	32MB	NA	8MB HypeRAM	POF assembled
TE0725-03-100-2I9	100_2i	REV03|REV02|REV01	NA	32MB	NA	8MB HypeRAM	NA
TE0725-03-35-2I	35_2i	REV03|REV02|REV01	NA	32MB	NA	8MB HypeRAM	NA

Table 4: Hardware Modules
Design supports following carriers:

Carrier Model	Notes

Table 5: Hardware Carrier
Additional HW Requirements:

Additional Hardware	Notes
TE0790 JTAG Programmer	It's not recommended to use TE0790 for power supply(TE0790 TRM[5])
External power supply	

Table 6: Additional Hardware

4.5 Content

For general structure and of the reference design, see Project Delivery - Xilinx devices[6]

4.5.1 Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
Vitis	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

Table 7: Design sources

4.5.2 Additional Sources

Type	Location	Notes
--	--	--

Table 8: Additional design sources

4.5.3 Prebuilt

5 https://wiki.trenz-electronic.de/display/PD/TE0790+TRM#TE0790TRM-PowerandPower-OnSequence
6 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices

File	File-Extension	Description
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
MCS-File	*.mcs	Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only)
MMI-File	*.mmi	File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems
SREC-File	*.srec	Converted Software Application for MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebult content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0725 "HyperRAM" Reference Design[7]

7 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/3.5x7.3/TE0725/Reference_Design/2019.2/HyperRAM

5 Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

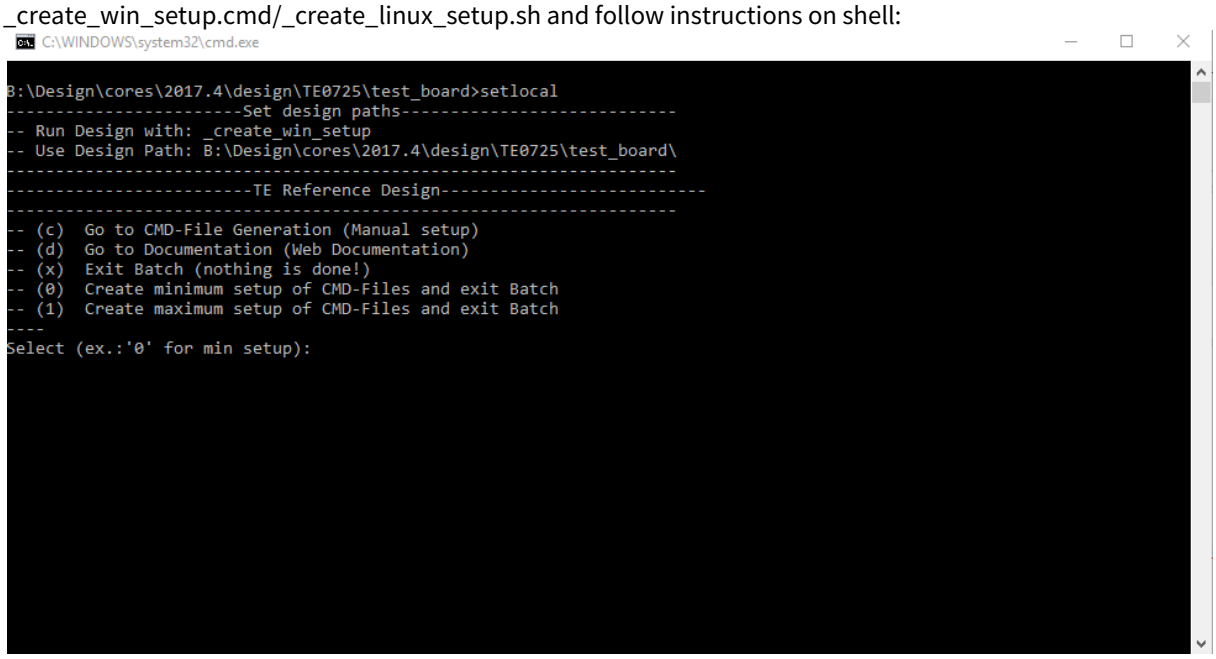
See also:

- Xilinx Development Tools[8]
- Vivado Projects - TE Reference Design[9]
- Project Delivery.[10]

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality[11]

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process)
   a. (optional for manual changes) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd" Note: Select correct one, see alsoTE Board Part Files[12]
5. Create XSA and export to prebuilt folder

8 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides
9 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design
10 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices
11 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality
12 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
      Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Generate Programming Files with Vitis
   a. Run on Vivado TCL: TE::sw_run_vitis -all
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv" App from Firmware folder will be add into BlockRAM. If you add other app, you must select *.elf manually on Vivado
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_vitis
      Note: TCL scripts generate also platform project, this must be done manuelly in case GUI is used. See Vitis[13]
7. Copy Application (memory_test.elf) into \firmware\microblaze_0\
   a. memory_test.elf or srec_spi_bootloader.elf
      Note only one elf shouldbe put into this folder
8. Regenerate Design:
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
      Note: App from Firmware folder will be add into BlockRAM. If you add other app, you must select *.elf manually on Vivado
   b. (alternative) Use SDK or Vivado to update generate Bitfile with new Application and regenerate mcs manually.

13 https://wiki.trenz-electronic.de/display/PD/Vitis

6 Launch

6.1 Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging[14]

6.1.1 Get prebuilt boot binaries

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection
   c. Select Create and open delivery binary folder
      Note: Folder (<project foler>/_binaries_<Artikel Name>) with subfolder (boot_<app name>) for different applications will be generated

6.1.2 QSPI

1. Connect JTAG and power on PCB
2. (if not done) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd" or open with "vivado_open_project_guimode.cmd", if generated.
3. Type on Vivado Console: TE::pr_program_flash
   Note: Alternative use SDK or setup Flash on Vivado manually
4. Reboot (if not done automatically)

6.1.3 SD

Not used on this Example.

6.1.4 JTAG

1. Connect JTAG and power on PCB
2. (if not done) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd" or open with "vivado_open_project_guimode.cmd", if generated.
3. Open Vivado HW Manager
4. Program Bitfile
   a. Note: Flash musst be configured with correct mcs file, in case srec_spi_bootloader.elf is used as app

14 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging

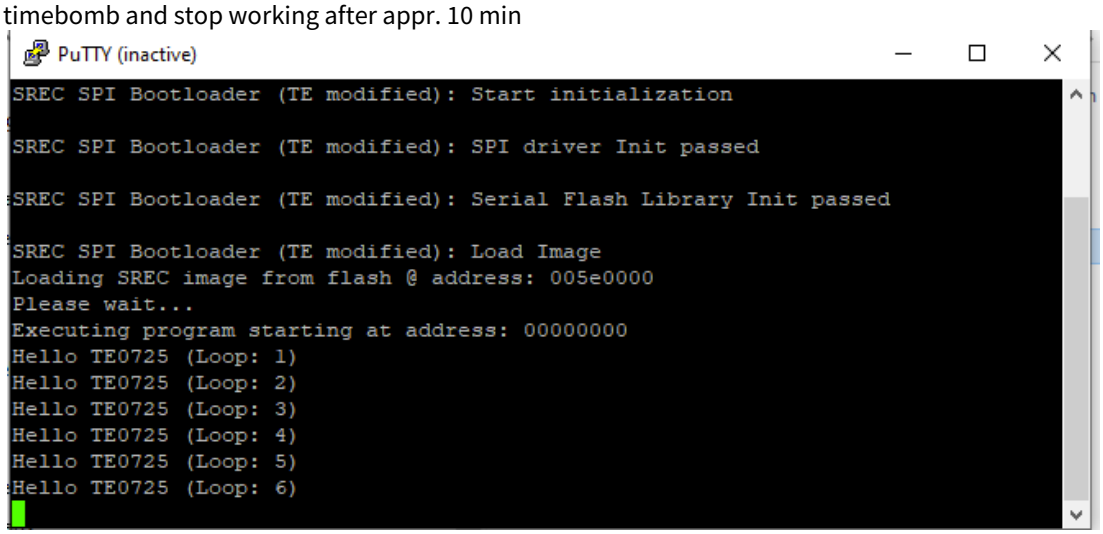
6.2 Usage

HBMC IP is a 10 minute run-time limited evaluation version of the full-edition

1. Prepare HW like described on section Programming(see page 13)
2. Connect UART USB (most cases same as JTAG)
3. Power On PCB (Do not restart, if you use Bitfile programming)
   Note: FPGA Loads Bitfile from Flash

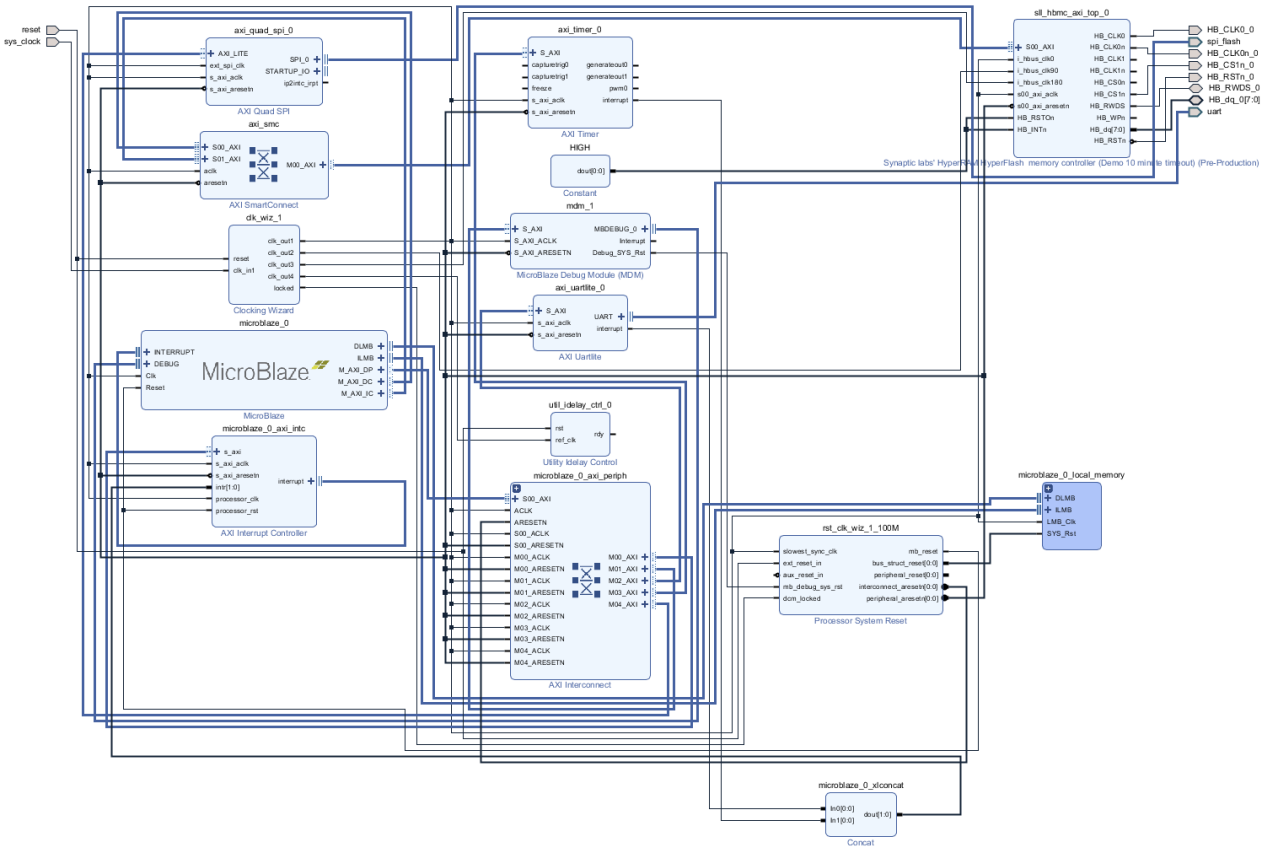
6.2.1 UART

1. Open Serial Console (e.g. putty)
   a. Speed: 9600
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Uart Console:
   Srec and Hello TE0725: Important, Hello TE0725 is running on Hyperam and Hyperram DEMO-IP has timebomb and stop working after appr. 10 min



7 System Design - Vivado

7.1 Block Design



7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 50 [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.M1PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M2PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M0PIN PULLNONE [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]
```

7.2.2 Design specific constrain

_i_hyperram.xdc

```
set_property PACKAGE_PIN A13 [get_ports HB_CLK0_0]
set_property PACKAGE_PIN A14 [get_ports HB_CLK0n_0]

set_property PACKAGE_PIN E17 [get_ports {HB_dq_0[0]}]
set_property PACKAGE_PIN B17 [get_ports {HB_dq_0[1]}]
set_property PACKAGE_PIN F18 [get_ports {HB_dq_0[2]}]
set_property PACKAGE_PIN F16 [get_ports {HB_dq_0[3]}]
set_property PACKAGE_PIN G17 [get_ports {HB_dq_0[4]}]
set_property PACKAGE_PIN D18 [get_ports {HB_dq_0[5]}]
set_property PACKAGE_PIN B18 [get_ports {HB_dq_0[6]}]
set_property PACKAGE_PIN A16 [get_ports {HB_dq_0[7]}]


set_property PACKAGE_PIN E18 [get_ports HB_RWDS_0]

set_property PACKAGE_PIN D17 [get_ports HB_CS1n_0]
set_property PACKAGE_PIN J17 [get_ports HB_RSTn_0]

#set_property PACKAGE_PIN A18 [get_ports HB_CS0n_0 ]
#set_property PACKAGE_PIN J18 [get_ports HB_INTn_0 ]
#set_property PACKAGE_PIN C17 [get_ports HB_RSTOn_0]


#
# FPGA Pin Voltage assignment
#
set_property IOSTANDARD LVCMOS18 [get_ports HB_CLK0_0]
set_property IOSTANDARD LVCMOS18 [get_ports HB_CLK0n_0]
set_property IOSTANDARD LVCMOS18 [get_ports {HB_dq_0[*]}]
set_property IOSTANDARD LVCMOS18 [get_ports HB_CS1n_0]
set_property IOSTANDARD LVCMOS18 [get_ports HB_RSTn_0]
set_property IOSTANDARD LVCMOS18 [get_ports HB_RWDS_0]

#set_property IOSTANDARD LVCMOS18 [get_ports HB_CS0n_0]
#set_property IOSTANDARD LVCMOS18 [get_ports HB_INTn_0]
#set_property IOSTANDARD LVCMOS18 [get_ports HB_RSTOn_0]

#set_property PULLUP true [get_ports HB_RSTOn_0]
#set_property PULLUP true [get_ports HB_INTn_0]

#
#Hyperbus Clock - change according to clk pin on PLL
#
create_generated_clock -name clk_0   -source [get_pins msys_i/clk_wiz_0/inst/
mmcm_adv_inst/CLKIN1] -master_clock sys_clock [get_pins msys_i/clk_wiz_0/inst/
mmcm_adv_inst/CLKOUT0]
```

```
create_generated_clock -name clk_90  -source [get_pins msys_i/clk_wiz_0/inst/
mmcm_adv_inst/CLKIN1] -master_clock sys_clock [get_pins msys_i/clk_wiz_0/inst/
mmcm_adv_inst/CLKOUT1]
create_generated_clock -name clk_180 -source [get_pins msys_i/clk_wiz_0/inst/
mmcm_adv_inst/CLKIN1] -master_clock sys_clock [get_pins msys_i/clk_wiz_0/inst/
mmcm_adv_inst/CLKOUT2]

#
#100Mhz clock freqeuncy - change accordingly
#
set hbus_freq_ns   10

set dqs_in_min_dly -0.5
set dqs_in_max_dly  0.5

set HB_dq_ports    [get_ports HB_dq_0[*]]

#
#Create RDS clock and RDS virtual clock
#
create_clock -period $hbus_freq_ns -name rwds_clk      [get_ports HB_RWDS_0]
create_clock -period $hbus_freq_ns -name virt_rwds_clk

#
#Input Delay Constraint -  HB_RWDS-HB_DQ
#
set_input_delay -clock [get_clocks virt_rwds_clk]             -max ${dqs_in_max_dly}
${HB_dq_ports}
set_input_delay -clock [get_clocks virt_rwds_clk] -clock_fall -max ${dqs_in_max_dly}
${HB_dq_ports} -add_delay

set_input_delay -clock [get_clocks virt_rwds_clk]             -min ${dqs_in_min_dly}
${HB_dq_ports} -add_delay
set_input_delay -clock [get_clocks virt_rwds_clk] -clock_fall -min ${dqs_in_min_dly}
${HB_dq_ports} -add_delay

set_multicycle_path -setup -end -rise_from [get_clocks virt_rwds_clk] -rise_to
[get_clocks rwds_clk] 0
set_multicycle_path -setup -end -fall_from [get_clocks virt_rwds_clk] -fall_to
[get_clocks rwds_clk] 0

set_false_path  -fall_from [get_clocks virt_rwds_clk] -rise_to [get_clocks rwds_clk]
-setup
set_false_path  -rise_from [get_clocks virt_rwds_clk] -fall_to [get_clocks rwds_clk]
-setup
set_false_path  -fall_from [get_clocks virt_rwds_clk] -fall_to [get_clocks rwds_clk]
-hold
set_false_path  -rise_from [get_clocks virt_rwds_clk] -rise_to [get_clocks rwds_clk]
-hold

set_false_path -from [get_clocks clk_0] -to [get_clocks rwds_clk]
set_false_path -from [get_clocks rwds_clk] -to [get_clocks clk_0]

#
#Output Delay Constraint -  HB_CLK0-HB_DQ
#
```

```
create_generated_clock -name HB_CLK0_0 -source [get_pins */*/*/U_IO/U_CLK0/dq_idx_[0]
.ODDR_inst/C] -multiply_by 1 -invert [get_ports HB_CLK0_0]

set_output_delay -clock [get_clocks HB_CLK0_0] -min -1.000 ${HB_dq_ports}
set_output_delay -clock [get_clocks HB_CLK0_0] -max  1.000 ${HB_dq_ports}
set_output_delay -clock [get_clocks HB_CLK0_0] -min -1.000 ${HB_dq_ports} -clock_fall
-add_delay
set_output_delay -clock [get_clocks HB_CLK0_0] -max  1.000 ${HB_dq_ports} -clock_fall
-add_delay


set_false_path -from [get_pins */*/*/U_HBC/*/dq_io_tri_reg/C] -to ${HB_dq_ports}

set_false_path -from * -to [get_pins */*/inst/*/i_iavs0_270_rstn_1_reg/CLR]
set_false_path -from * -to [get_pins */*/inst/*/i_iavs0_270_rstn_2_reg/CLR]
set_false_path -from * -to [get_pins */*/inst/*/i_iavs0_270_rstn_3_reg/CLR]
```

8 Software Design - Vitis

For SDK project creation, follow instructions from:

Vitis[15]

8.1 Application

Template location: ./sw_lib/sw_apps/

8.1.1 srec_spi_bootloader

TE modified 2019.2 SREC

Bootloader to load app or second bootloader from flash into DDR

Descriptions:

- Modified Files: blconfig.h, bootloader.c
- Changes:
    - Add some console outputs and changed bootloader read address.
    - Add bugfix for 2018.2 qspi flash (some reinitialisation)

8.1.2 xilisf_v5_14

TE modified 2019.2 xilisf_v5_14

- Changed default Flash type to 5.

8.1.3 memory_test

Xilinx default memory test.

15 https://wiki.trenz-electronic.de/display/PD/Vitis

9 Additional Software

No additional software is needed.

10 Appx. A: Change History and Legal Notices

10.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2021-07-06	v.9[16]	@ John Hartfiel[17]	• update block design image
21-07-17	v.8	John Hartfiel	• new overview description
2020-04-29	v.7	John Hartfiel	• Design SW update with SREC Bootloader
2020-04-27	v.5	John Hartfiel	• 2019.2 update • Documentation style update
2018-08-09	v.4	John Hartfiel	• 2018.2 update
2018-06-06	v.3	John Hartfiel	• Documentation update
2018-06-05	v.2	John Hartfiel	• 2017.4 release
	All	@ John Hartfiel[18], Waldemar Hanemann[19]	

Table 10: Document change history.

16 https://wiki.trenz-electronic.de/pages/viewpage.action?pageId=162172554
17 https://wiki.trenz-electronic.de/display/~j.hartfiel
18 https://wiki.trenz-electronic.de/display/~j.hartfiel
19 https://wiki.trenz-electronic.de/display/~w.hanemann

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10.9 REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH[20]. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List[21] are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA)[22].

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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20 http://guidance.echa.europa.eu/
21 https://echa.europa.eu/candidate-list-table
22 http://www.echa.europa.eu/